REMARKS

In response to the Office Action mailed June 3, 2004, Applicant respectfully requests reconsideration. Claims 1-9 are currently pending in this application. Claims 2-4 and 7-9 are allowed. Claim 6 is indicated to be allowable with respect to its dependency from claim 2, but objected to with respect to its dependency from claim 5. Claim 10 is newly added. The application as presented is believed to be in condition for allowance.

Claim 6 is amended herein to remove its dependency from claim 5. Claim 6 now depends only from claim 2. Thus, it is respectfully requested that the objection to claim 6 based on its dependency from claim 5 be withdrawn. Claim 10 is newly added in this application to rewrite previously-pending claim 6 in independent form, with respect to its dependency from claim 5. Because claim 6 previously depended from claim 5 prior to this amendment, no new issues that would require further search or consideration are raised by the addition of claim 10.

The Office Action rejected claims 1 and 5 under 35 U.S.C. §102(b) as being purportedly unpatentable over Hall (5,175,828). Applicants respectfully traverse this rejection.

Claim 1

Claim 1 is directed to a method of operating a target computer system, wherein said target computer system has a memory comprising plural addressable locations and is adapted to run an application. The method comprises: providing on a host computer a file, comprising a subroutine required for operating of said application; dynamically loading said file from said host computer to said memory of said target computer system, whereby said file has an entry point at a dynamically-determined addressable location; storing at a predetermined one of said addressable locations data representative of the address of said entry point; running said application, whereby said application determines said data representative of said address thereby accessing said subroutine; and running said subroutine.

In Applicant's response filed April 15, 2004, Applicant explained that Hall does not disclose or suggest, "storing at a predetermined one of said addressable locations data representative of the address of said entry point," as recited in claim 1. Specifically, Applicant pointed out that in Hall, both the new subprogram and the jump table that specifies the RAM address of the new subprogram are stored in RAM and Hall does not teach or suggest that the

location of the jump table in RAM is predetermined. Thus, the location of the jump instruction to the new subprogram in the jump table may vary in dependence on the location of the jump instruction that is being modified or replaced. Therefore, the RAM address location of the jump instruction that specifies a jump to the RAM address of the new subprogram is not predetermined.

The Office Action agrees that Hall does not explicitly disclose storing, at a predetermined one of said addressable locations, data representative of the address of said entry point. However, the Office Action asserts that this limitation of claim 1 is inherent in Hall. Specifically, the Office Action asserts that "[t]he procedure calls to this new subroutine location address must be known by the calling procedures and, therefore, it is inherent that the address of the subroutine is predetermined as to allow the correct entry point calls to the subroutine." See Office Action, page 4, lines 10-13. Applicants respectfully disagree with this assertion.

Applicants agree that Hall discloses that the routine _jump_selectMeas(in application) is placed in RAM at a particular address. Applicants further agree that procedures calling this routine determine the RAM address of this routine when calling it. However, the RAM address of this routine is not predetermined. Instead, Hall discloses that the address of this routine is stored in a jump table. The jump table is also stored in RAM and is therefore modifiable. (Hall, lines 19-25). The RAM address of the routine is determined by looking up the address in this jump table. When the new subroutine _jump_selectMeas(in application) is placed in RAM, the jump table is modified to reflect the RAM address at which the routine is placed. (Hall, lines 30-37).

Thus, in Hall, the new routine _jump_selectMeas(in application) is not placed at a predetermined location. Instead, the routine may be placed at any location in RAM. Once the routine is placed at a particular RAM address, the jump table may be modified to reflect the new address at which the routine is located. Thus, it is not inherent in Hall that the address of the new subroutine is predetermined, as Hall discloses that the system operates in a manner where the subroutine address is not predetermined.

In addition, Hall is directed to dynamic linking, as opposed to dynamic loading. Hall discloses that a new procedure may be dynamically linked into the application, but only if the procedure has already been created and loaded onto the target computer. Thus, Hall also fails to

disclose or suggest, "dynamically loading said file from said host computer to said memory of said target computer system," as recited in claim 1.

In view of the foregoing, claim 1 patentably distinguishes over Hall. Therefore, it is respectfully requested that the rejection of claim 1 under 35 U.S.C. §102(b) be withdrawn.

Claim 5

Claim 5 is directed to a device for operating an embedded digital signal processor, said embedded signal processor having a memory comprising plural addressable locations, and being adapted to run an application. The device comprises a host computer connected to said embedded digital signal processor, said host computer comprising a computer file including a subroutine required for said application. The host computer comprises a linker-loader connected to said link and operative to send said file and dynamically load said file to said memory of said embedded signal processor whereby said file has an entry point at one of said addressable locations, said linker-loader comprising means for storing at a predetermined one of said addressable locations data representative of the address of said entry point. The embedded digital signal processor comprises processor circuitry running said application whereby said application determines said data representative of said address, thereby accessing said file to enable said application to run.

As should be clear from the discussion above, Hall does not teach or suggest "a linker-loader comprising means for storing at a predetermined one of said addressable locations data representative of the address of said entry point," as recited in claim 5.

Thus, claim 5 patentably distinguishes over Hall. Accordingly, it is respectfully requested that the rejection of claim 5 under 35 U.S.C. §102(b) be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

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Docket No.: S1022.80617US00
Date: October 4, 2004